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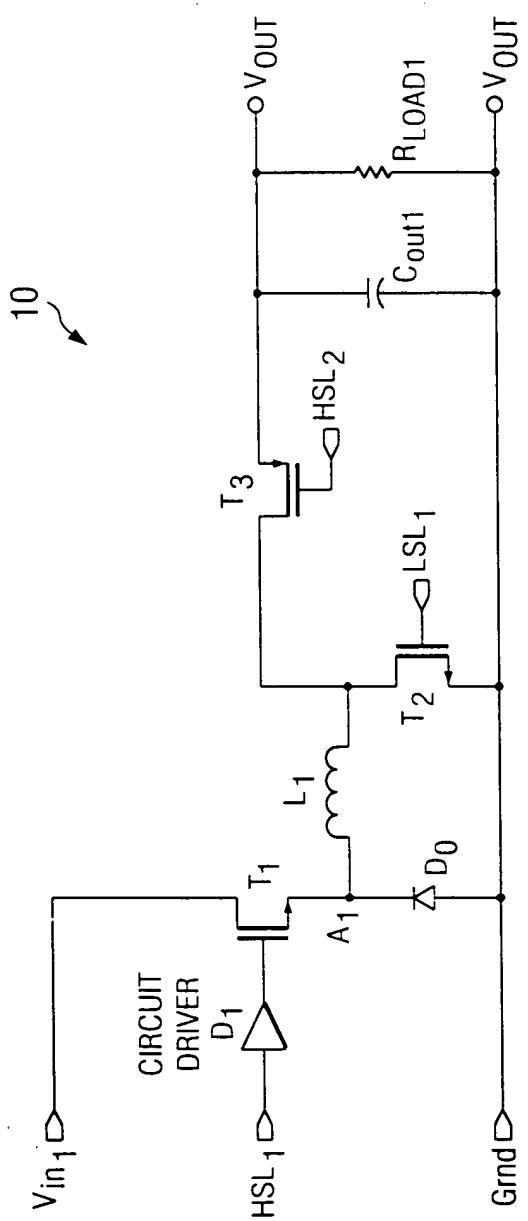


FIG. 1
(PRIOR ART)

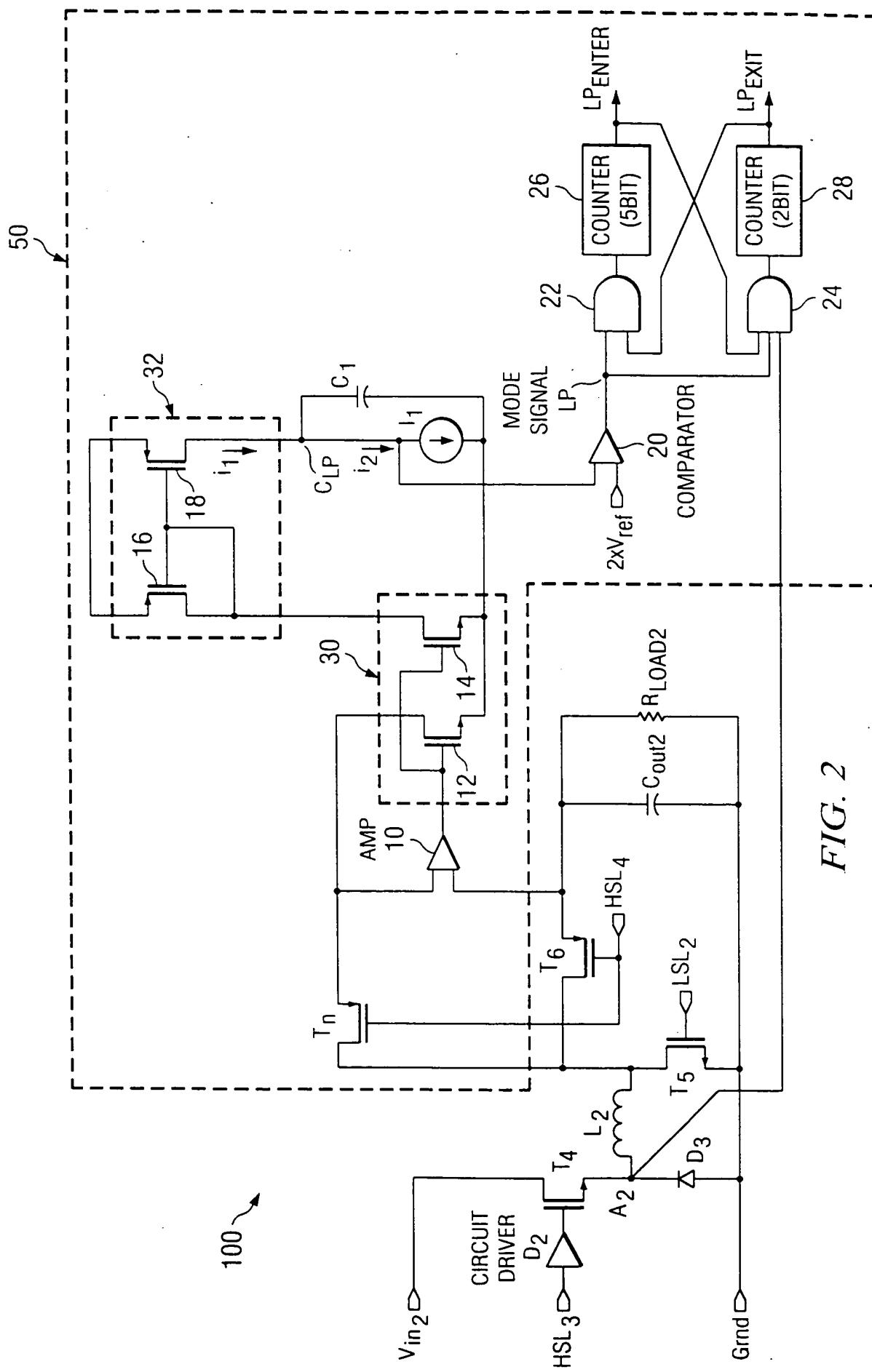
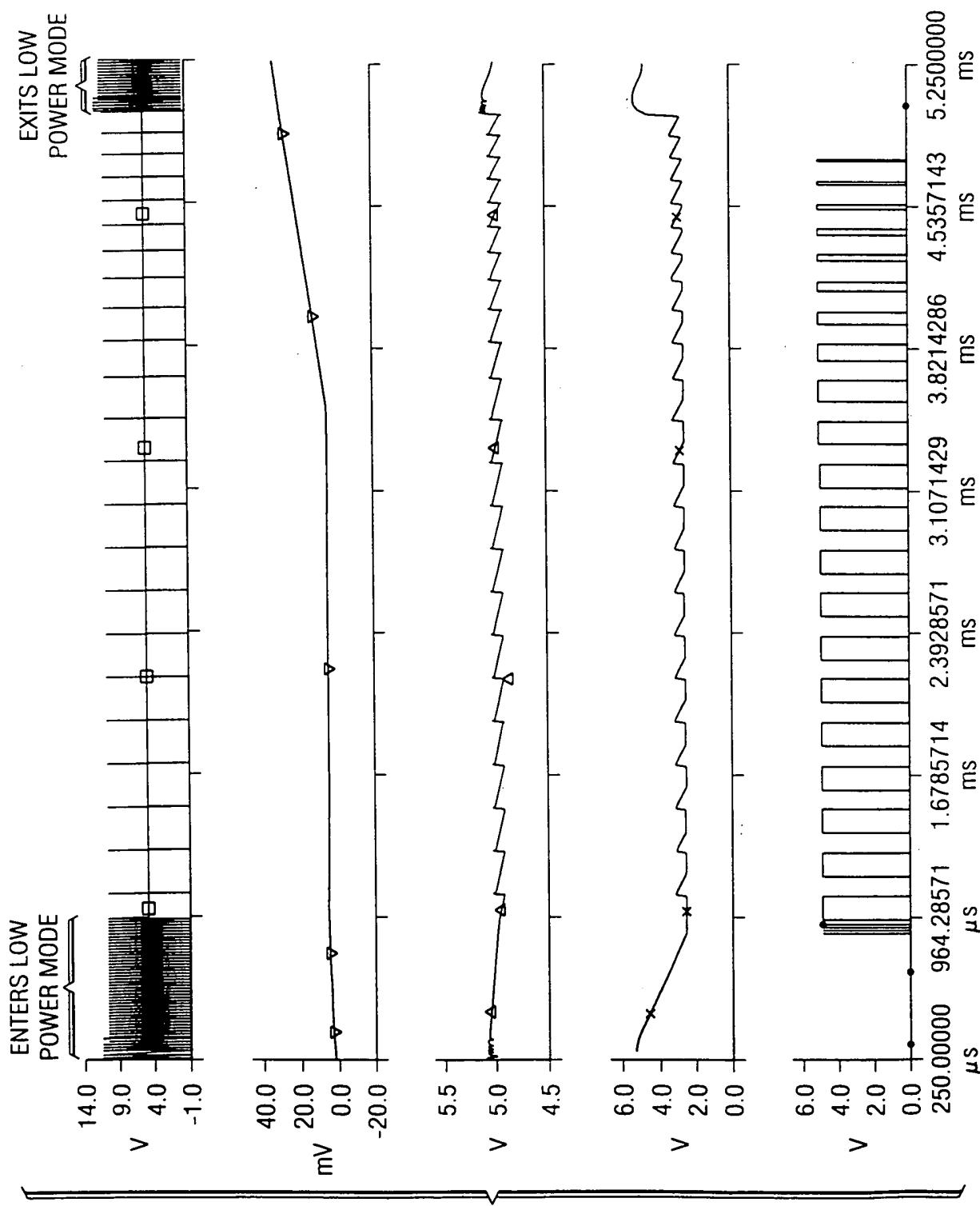


FIG. 2

FIG. 3

□ A_2 - SWITCHING NODE
 ▽ OUTPUT CURRENT
 ▲ OUTPUT VOLTAGE
 × CLP PIN
 • LOW POWER MODE SIGNAL



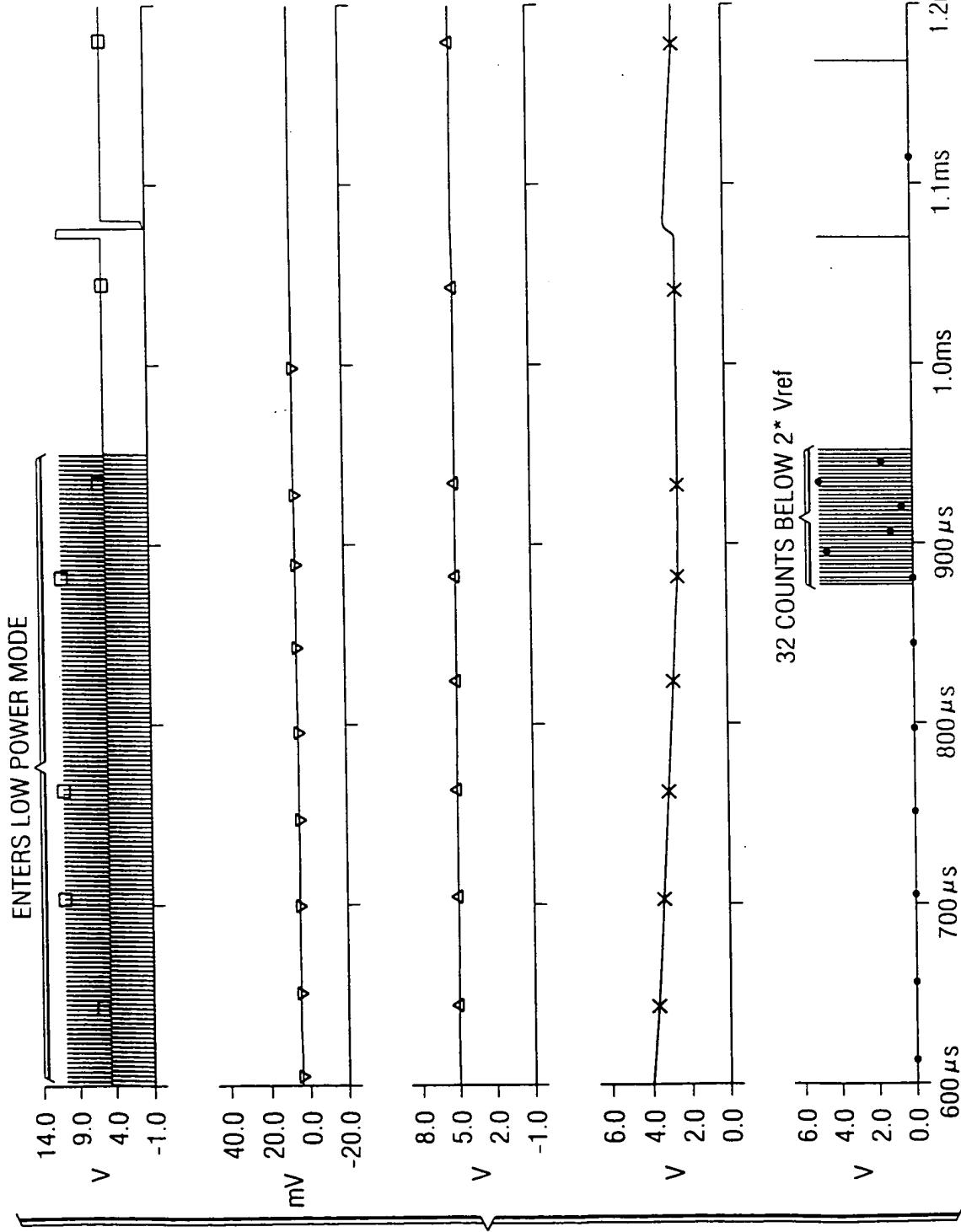


FIG. 5

